

FIG. 1
 (PRIOR ART)

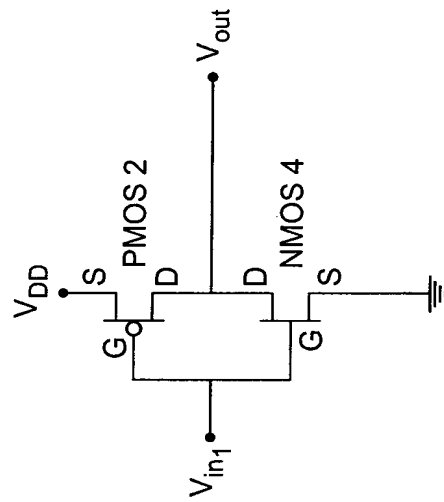


FIG. 2
 (PRIOR ART)

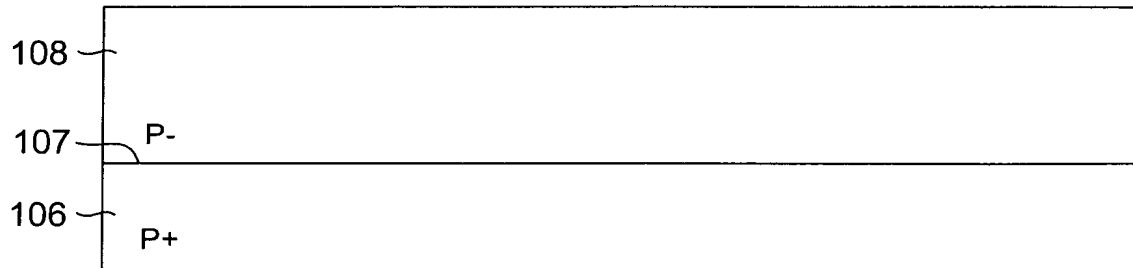


FIG. 3

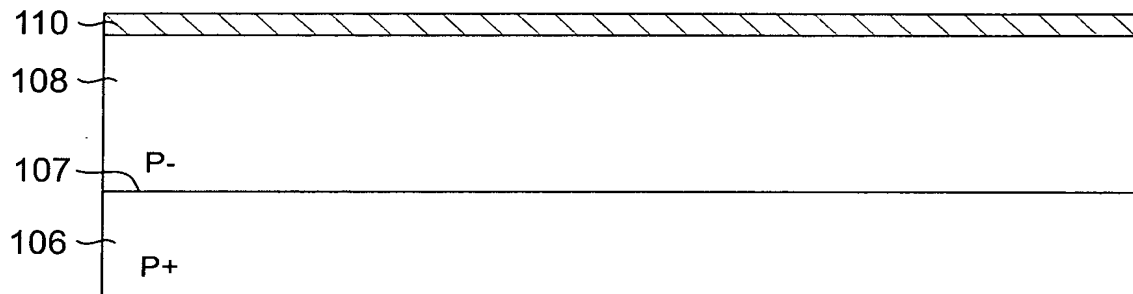


FIG. 4

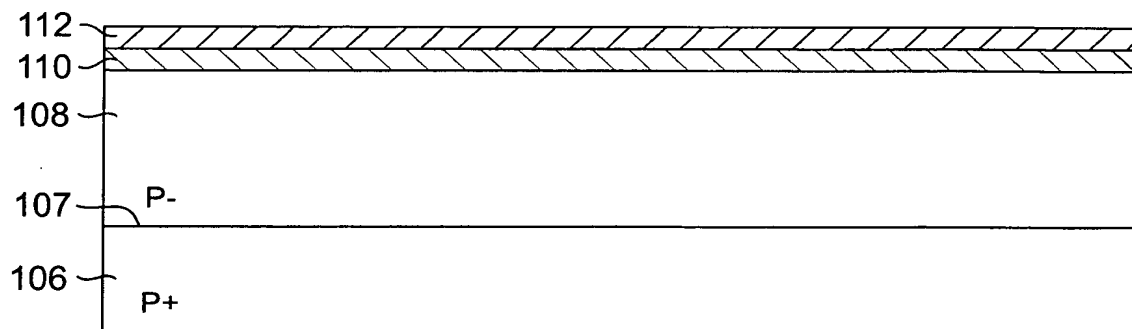


FIG. 5

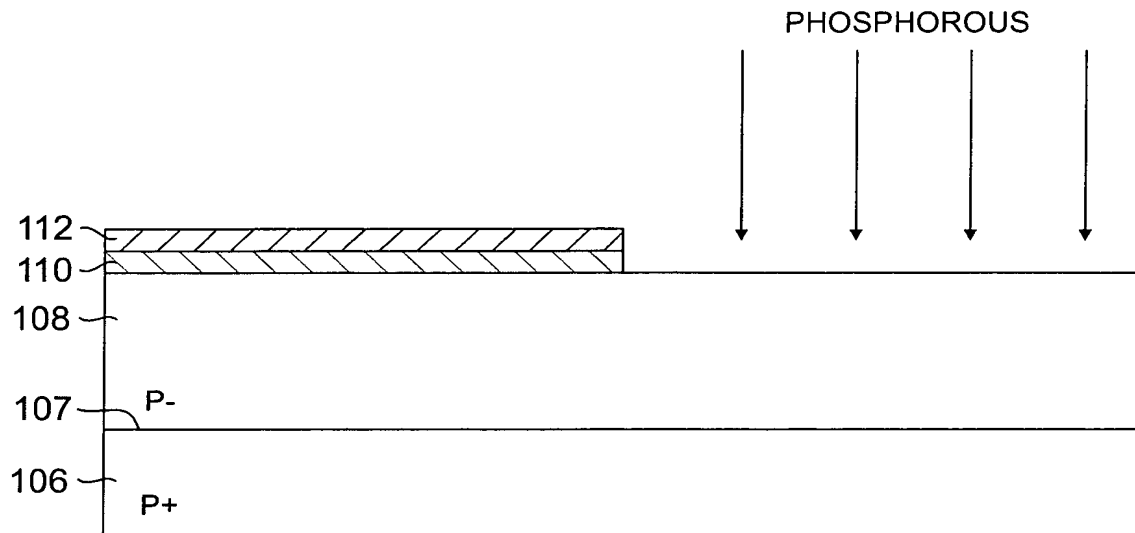


FIG. 6

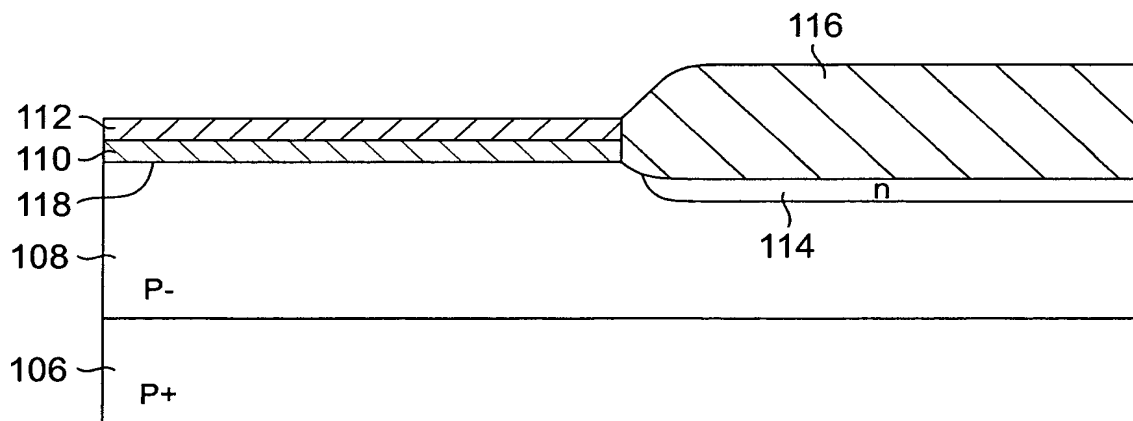


FIG. 7

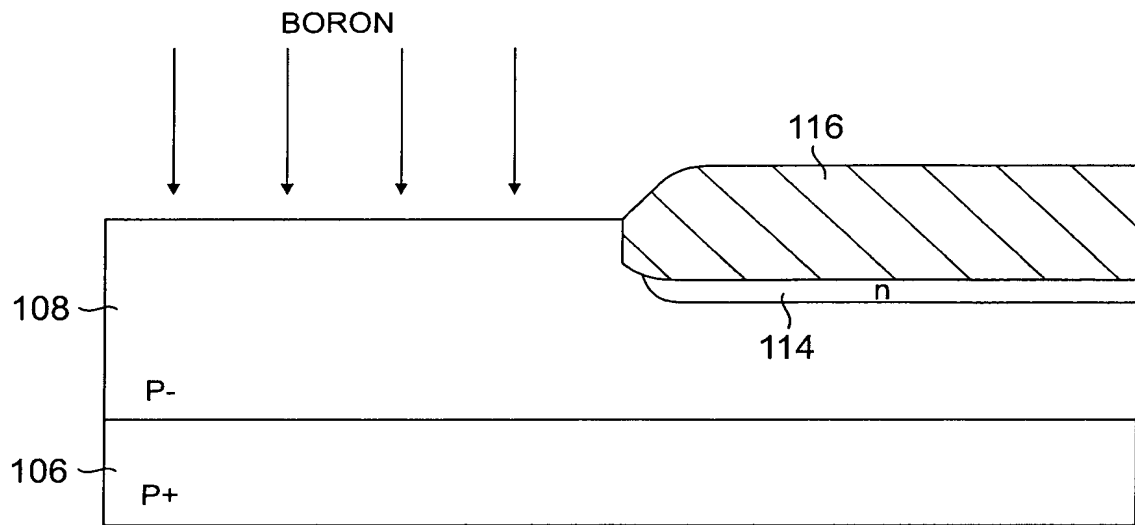


FIG. 8

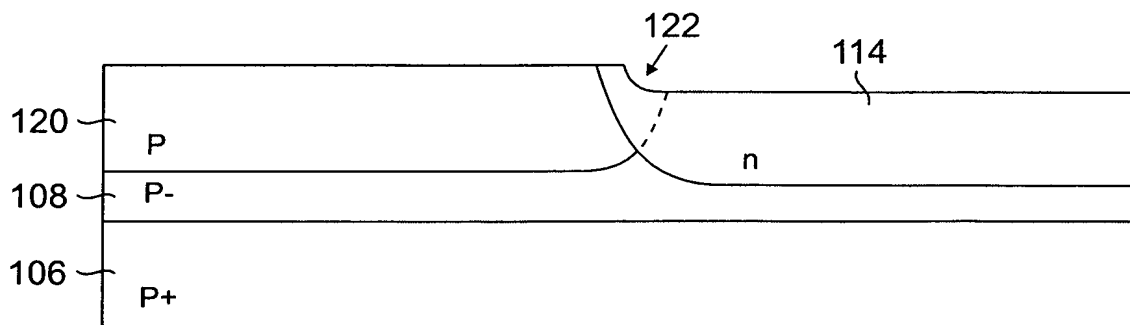


FIG. 9

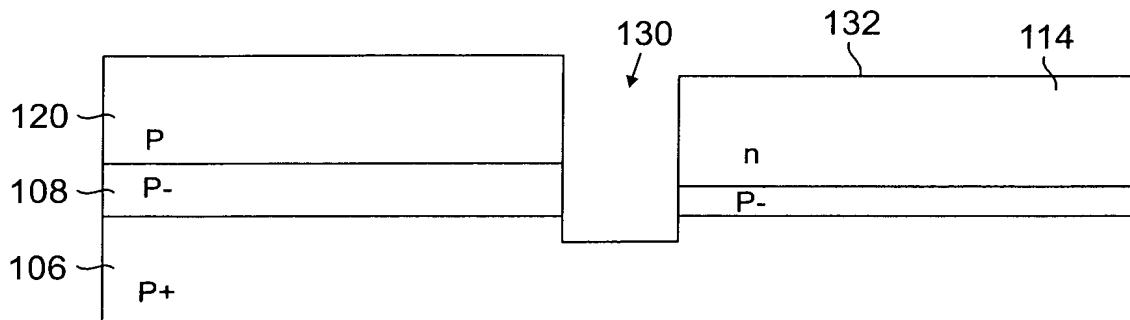


FIG. 10

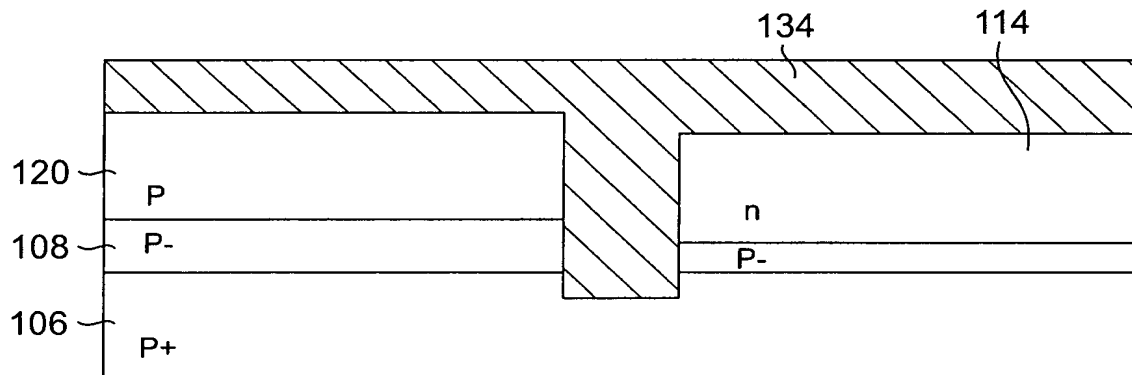


FIG. 11

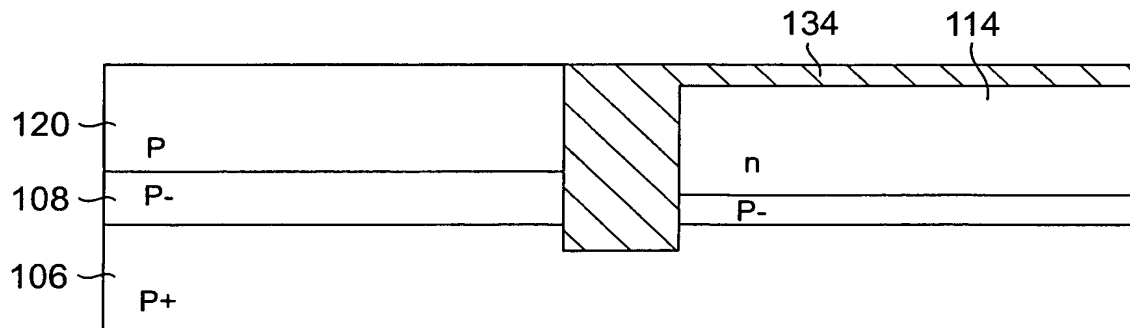


FIG. 12

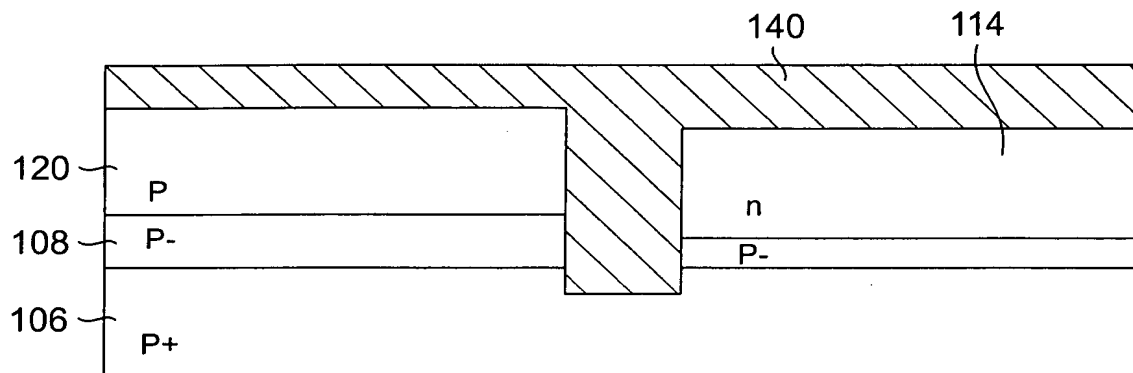


FIG. 13

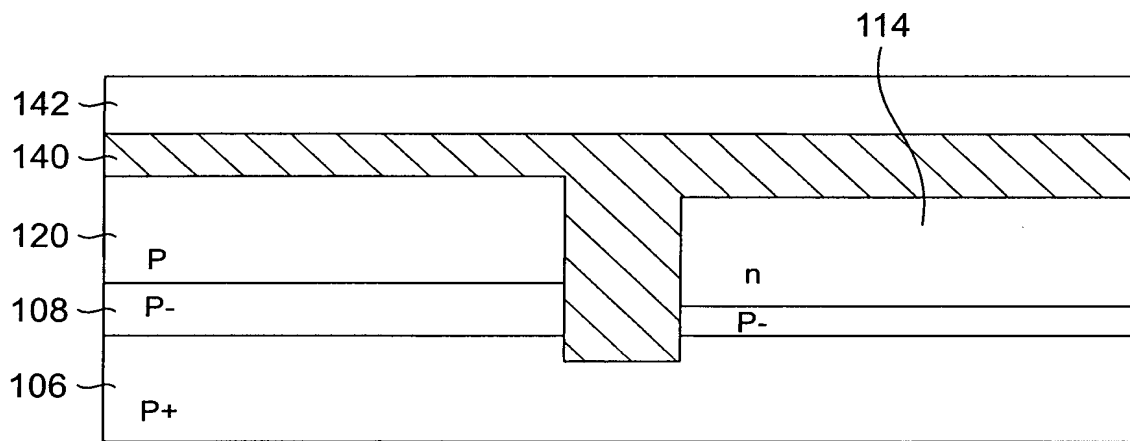


FIG. 14

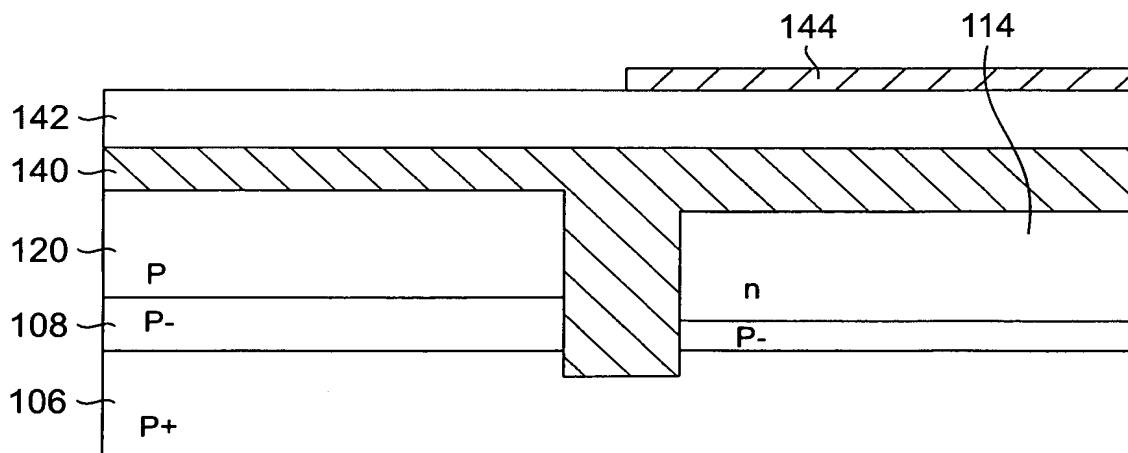
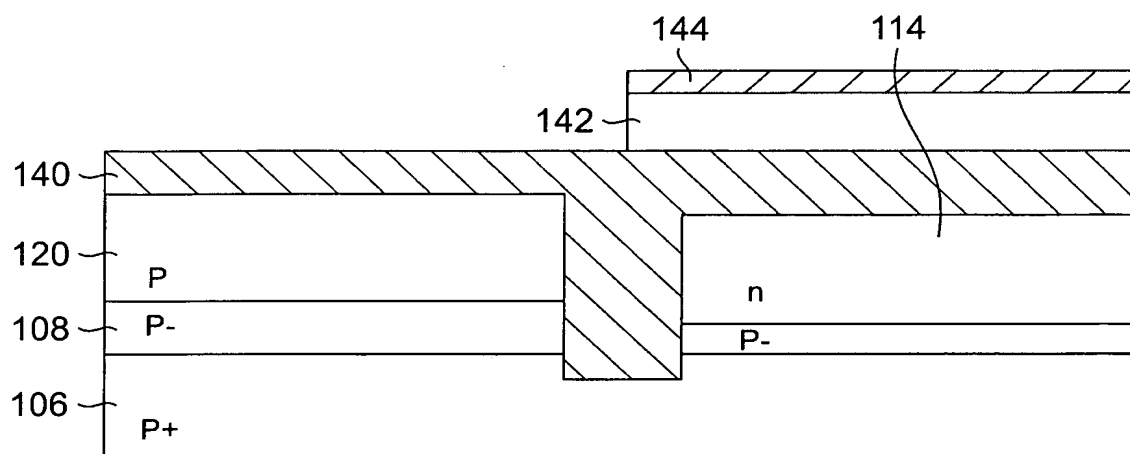


FIG. 15



A cross-sectional view of a semiconductor device. The device features a substrate with a P+ region (106) at the bottom, followed by a P- region (108). Above the P- region is a layer labeled 120, which contains a P region. A central structure, labeled 114, is formed on the P- region and extends upwards through the P region and layer 120. This central structure is composed of a bottom layer (140) and a top layer (142). The top layer (142) is further divided into a bottom portion (144) and a top portion (146). The top portion (146) is a thin layer that covers the top surface of the device. The bottom portion (144) is a thicker layer that is part of the central structure. The P- region (108) is also labeled as P-.

FIG. 17

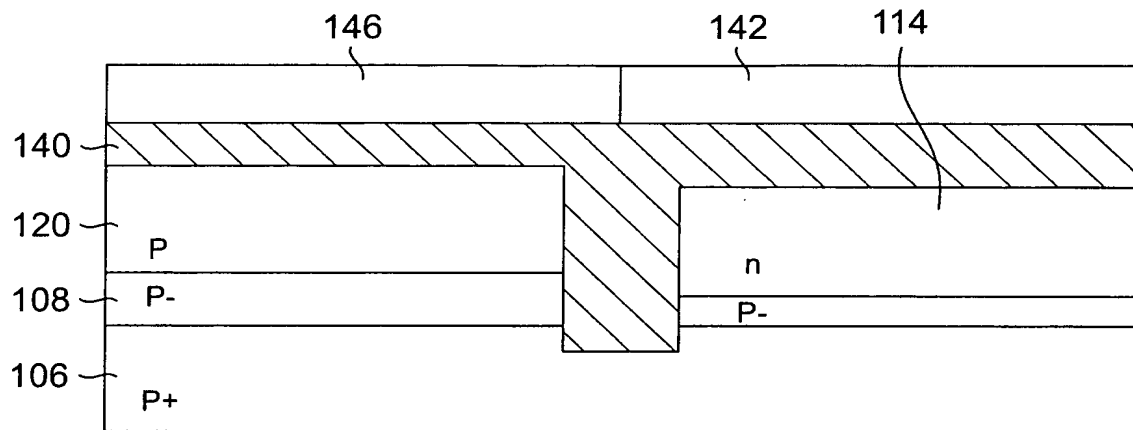


FIG. 18

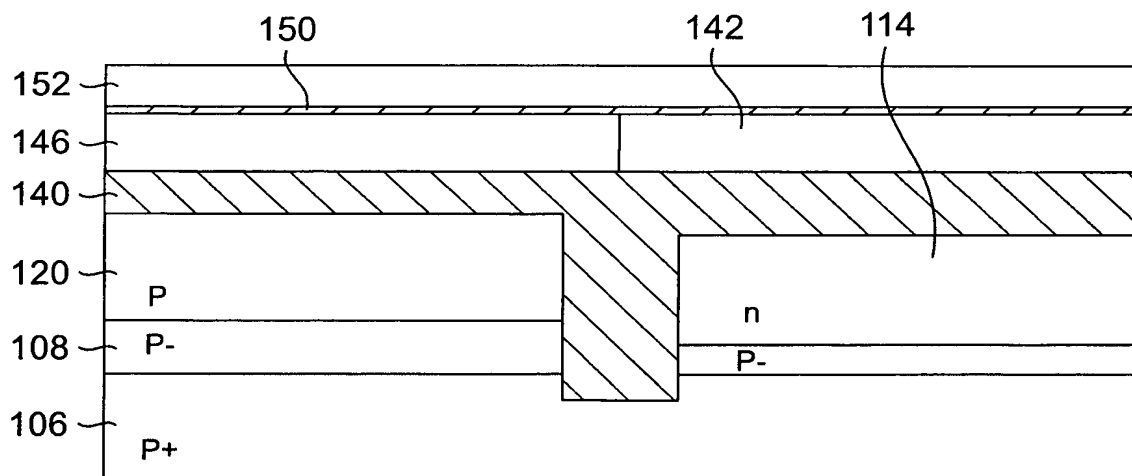


FIG. 19

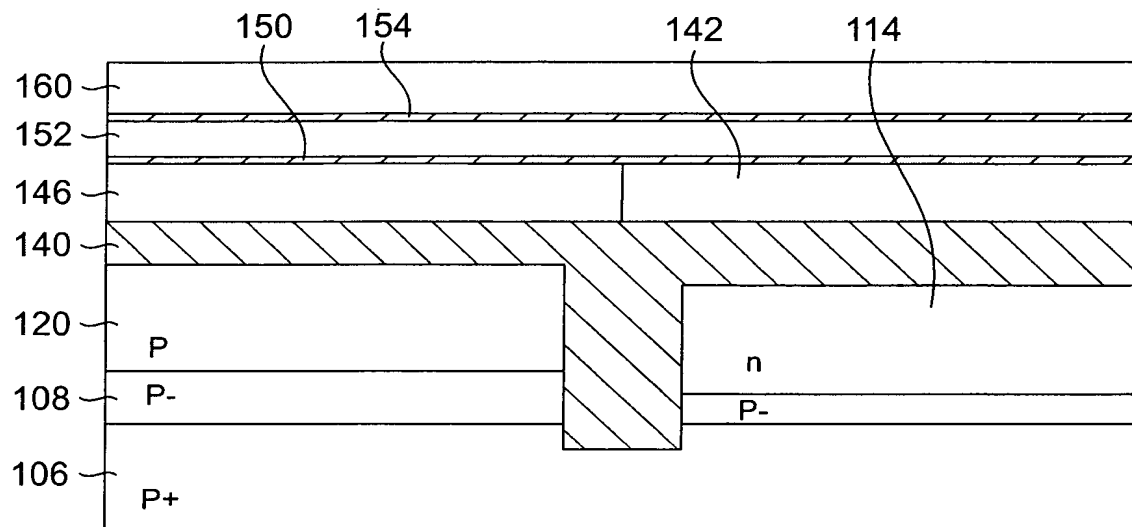


FIG. 20

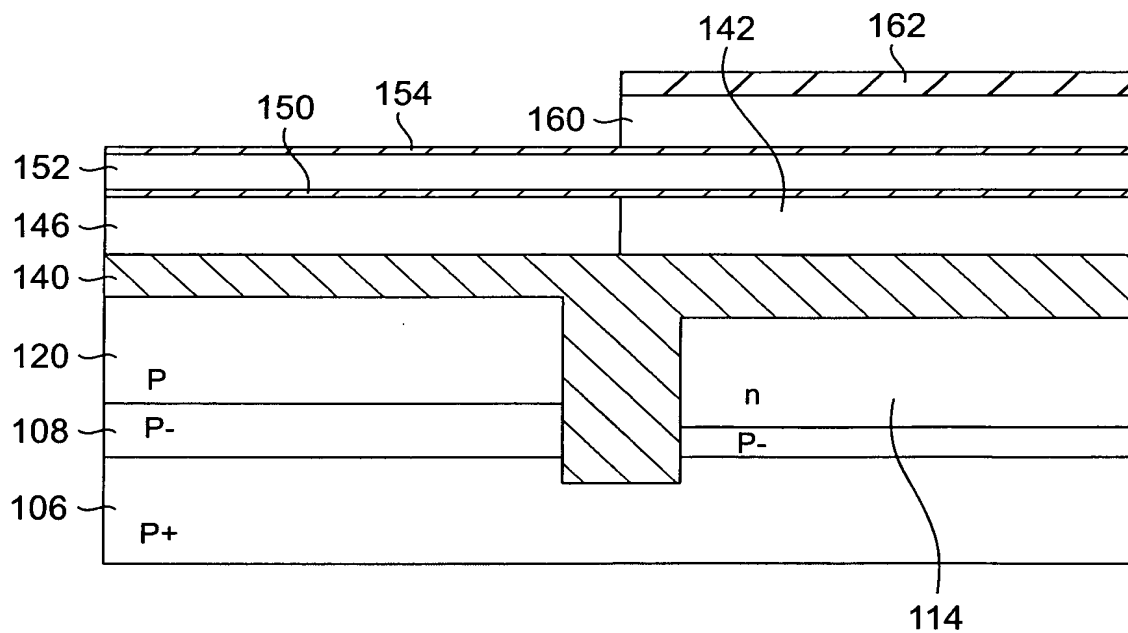


FIG. 21

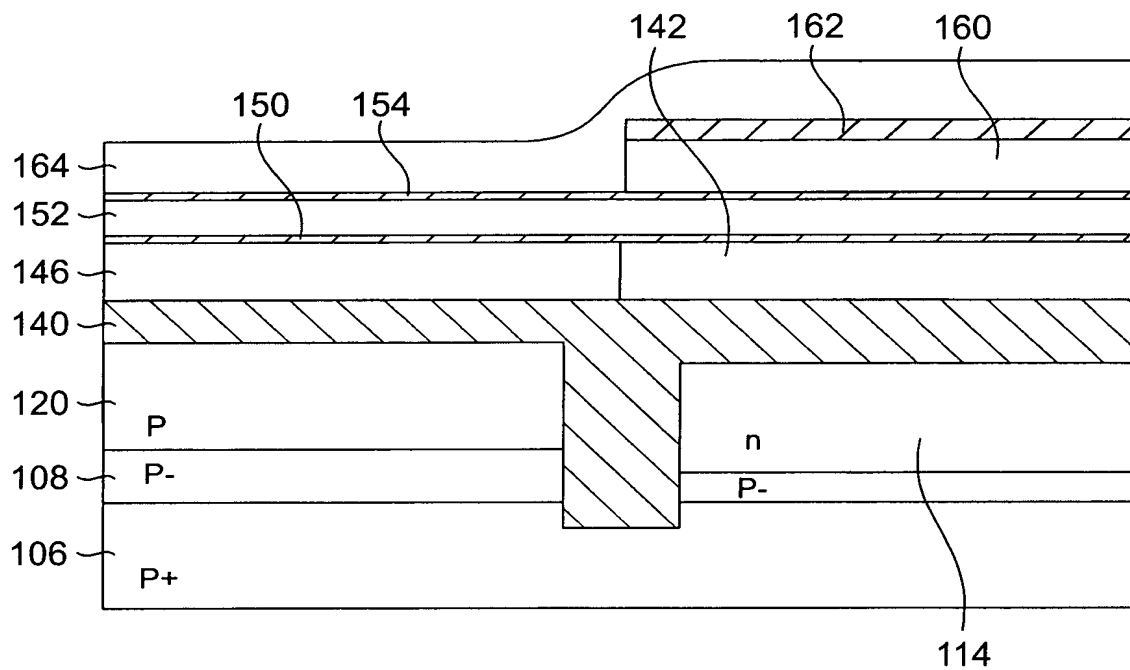


FIG. 22

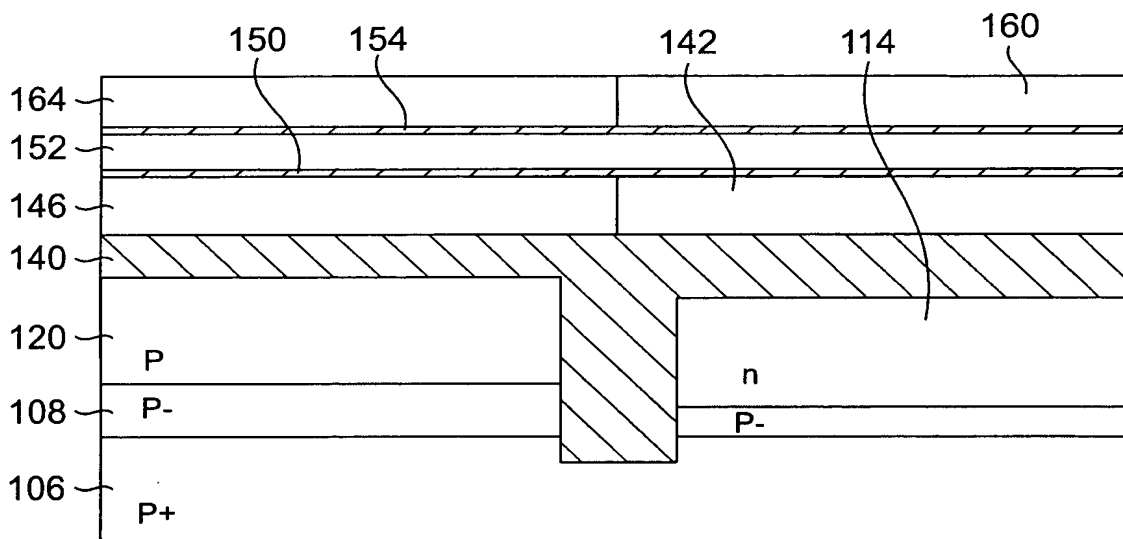


FIG. 23

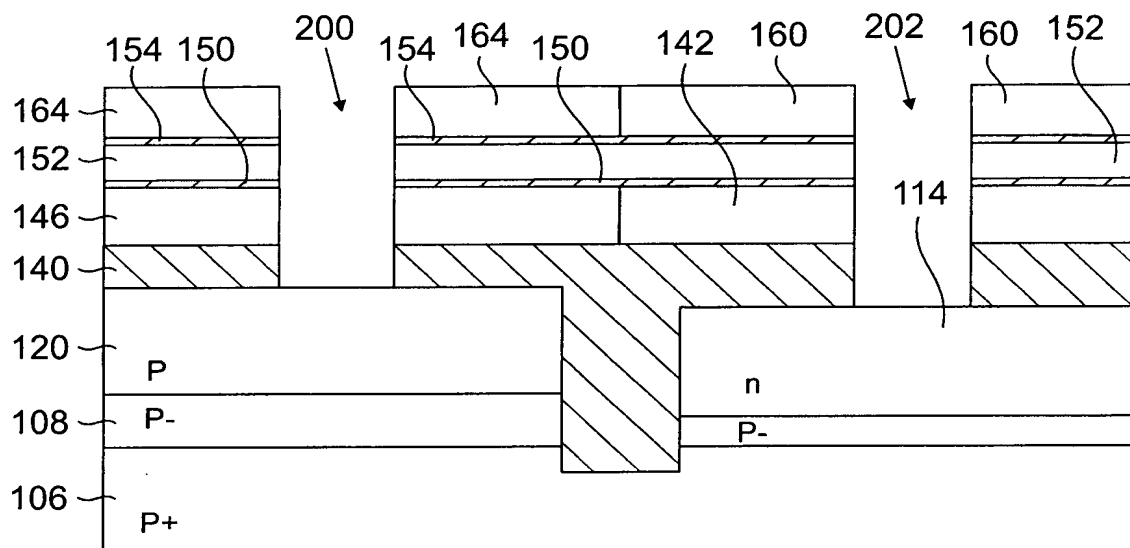


FIG. 24

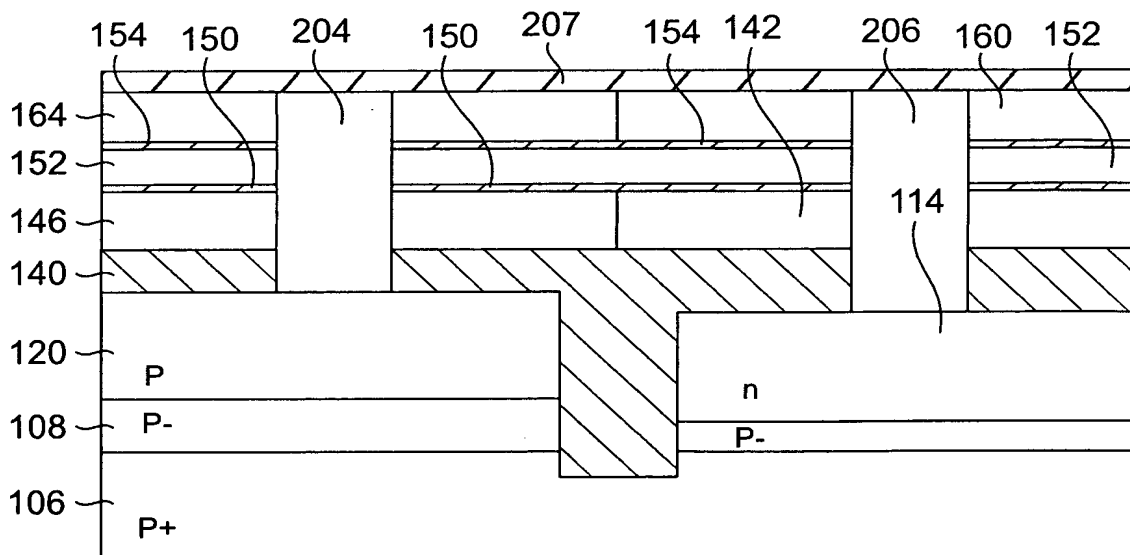


FIG. 25

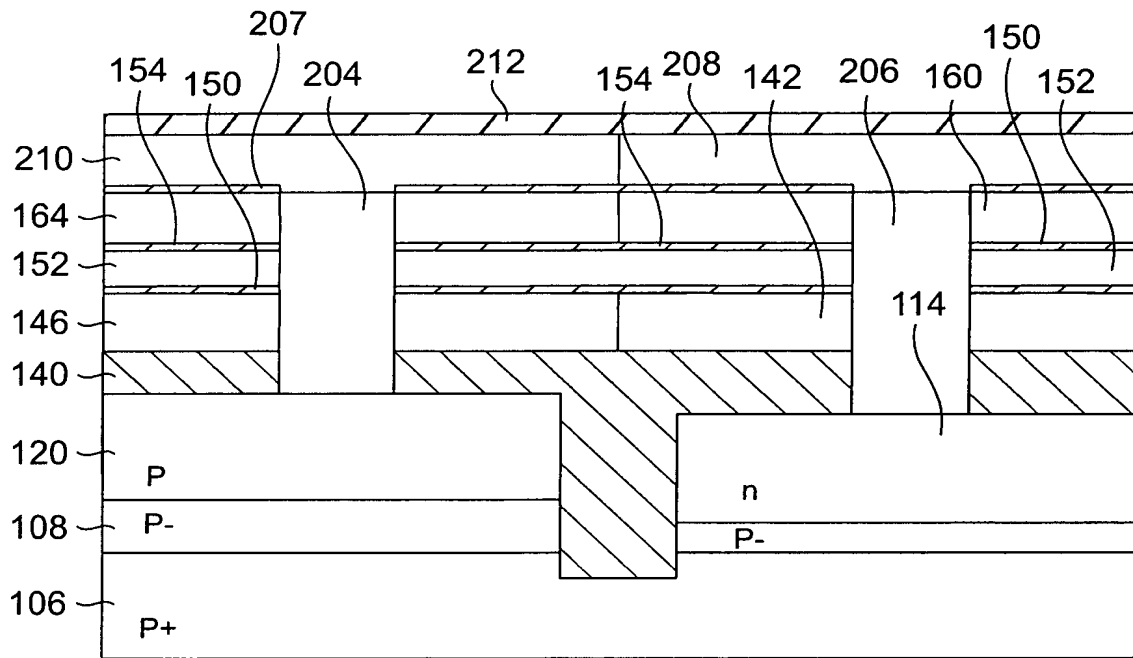


FIG. 26

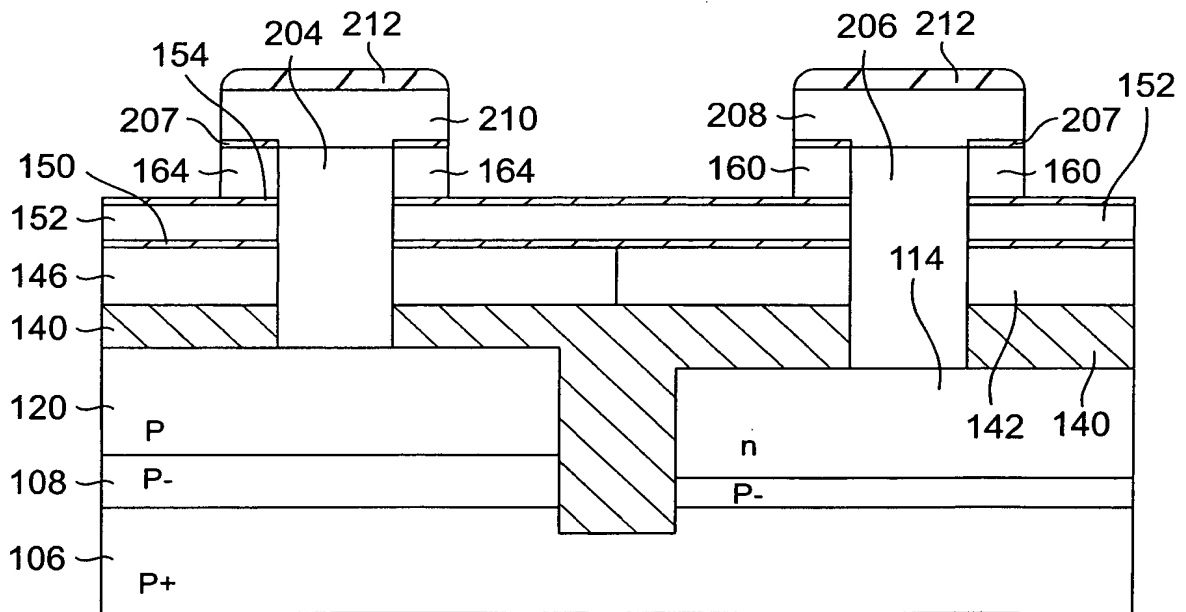


FIG. 27

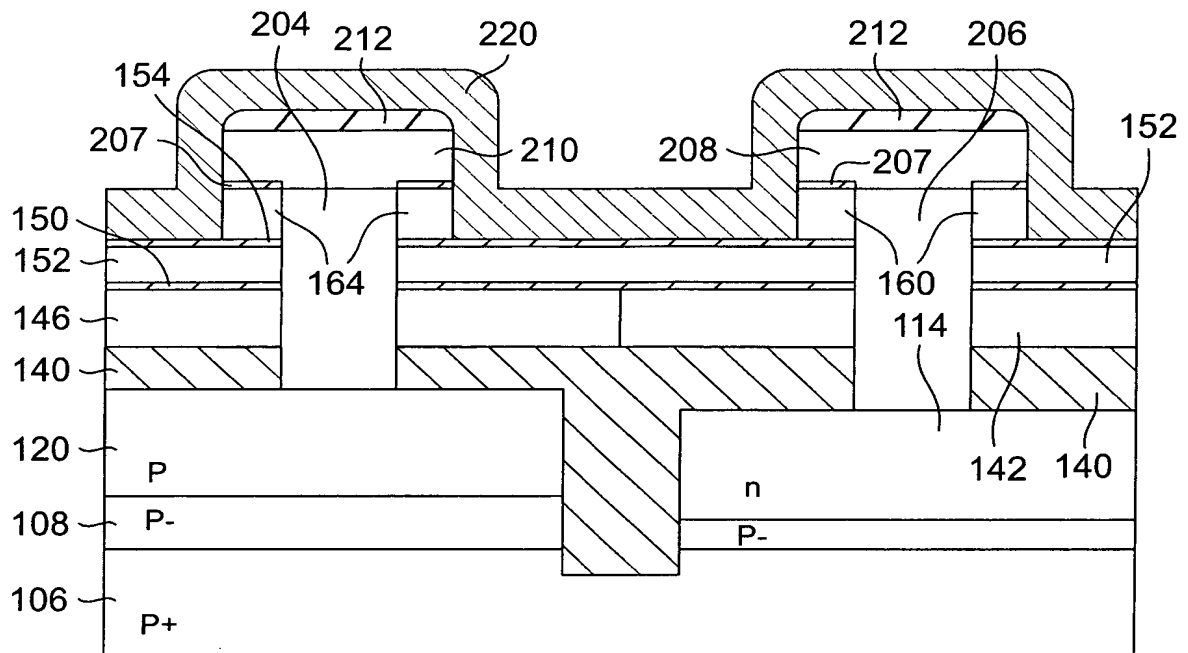


FIG. 28

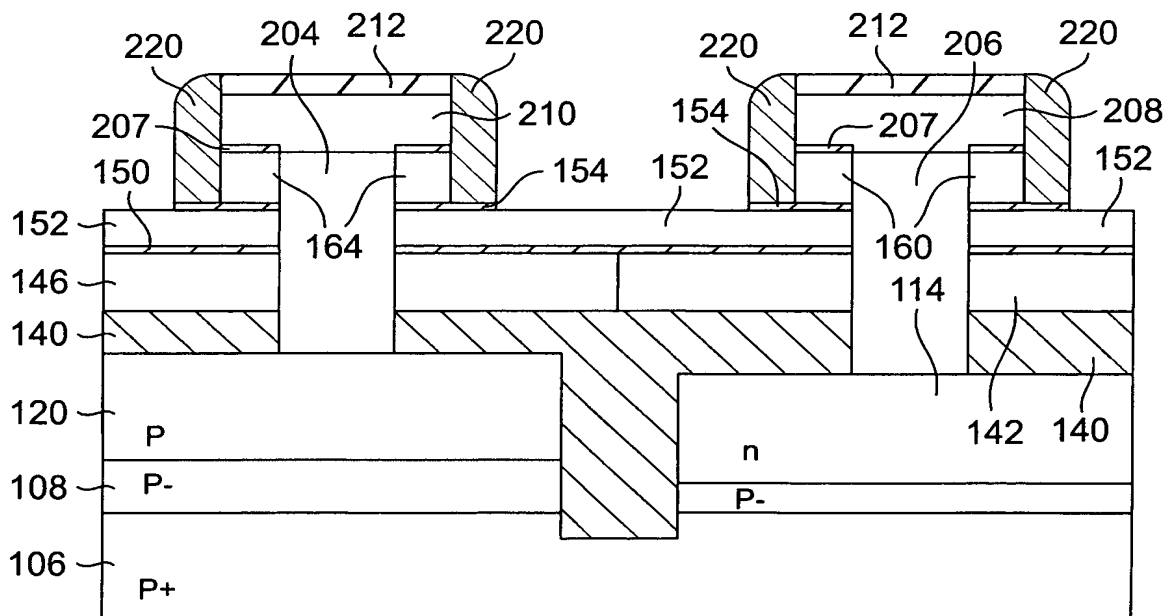


FIG. 29

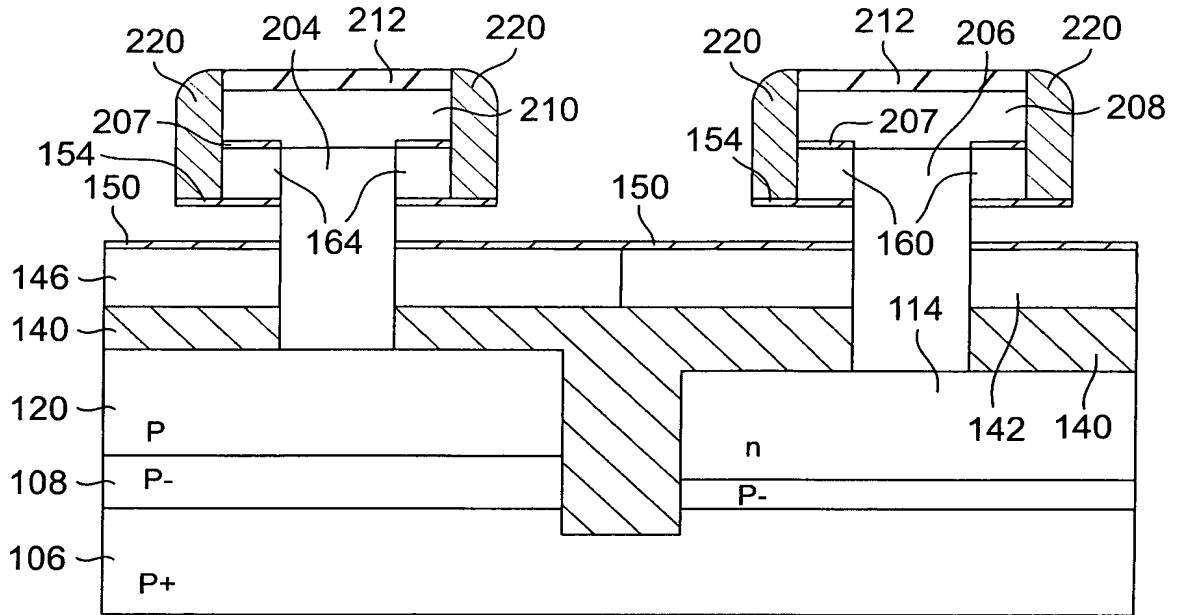


FIG. 30

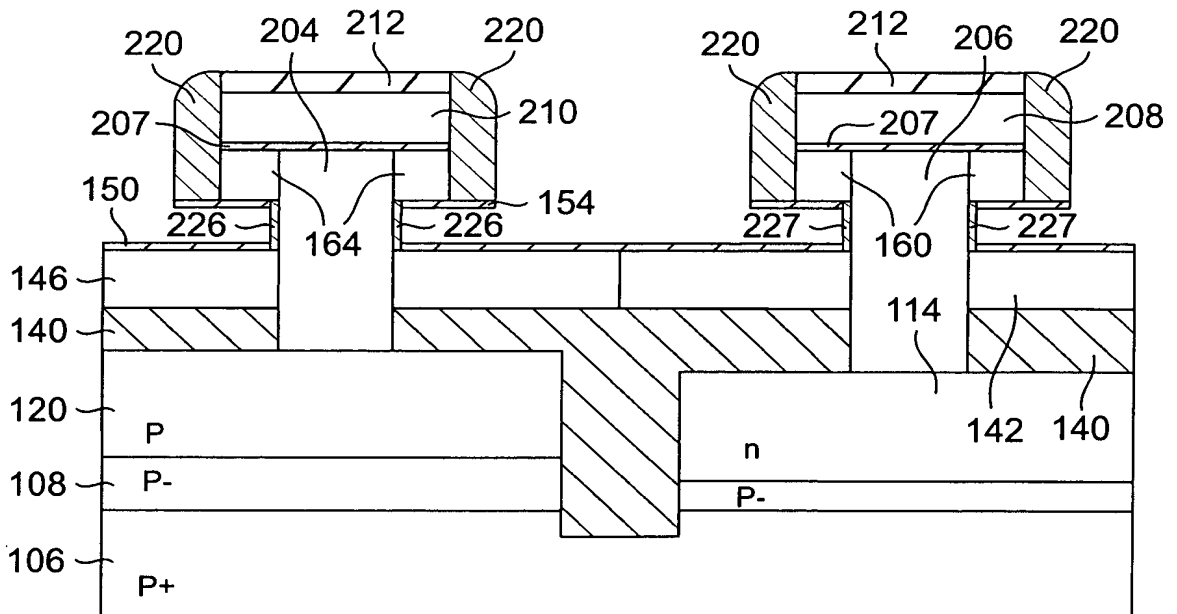


FIG. 31

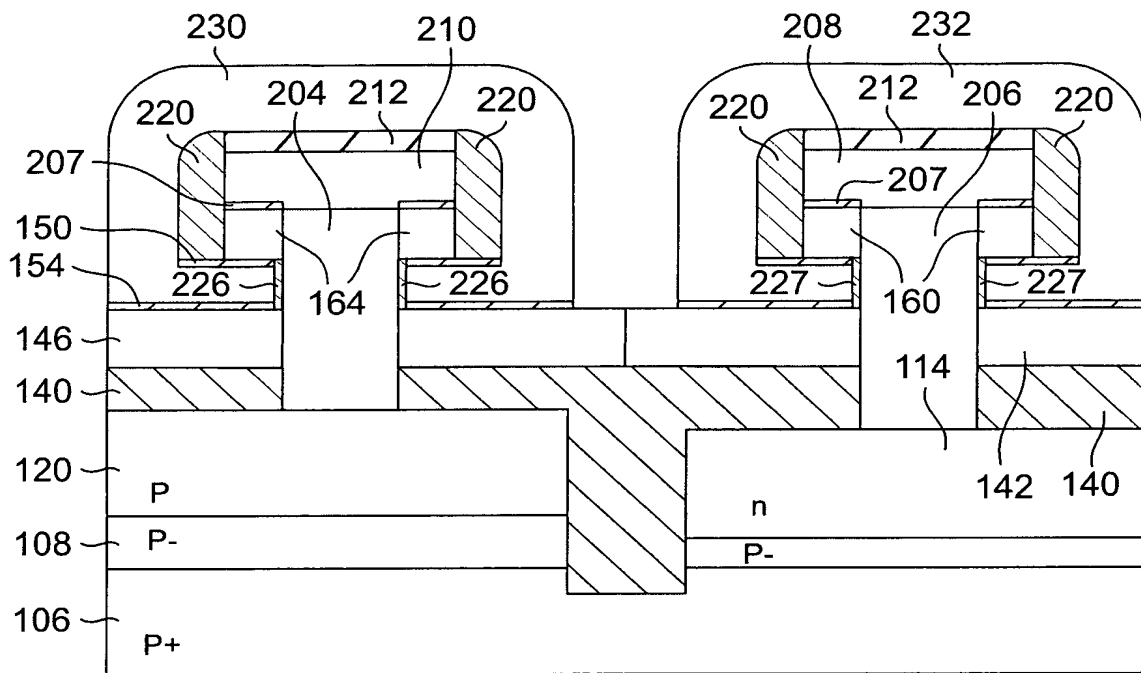


FIG. 32

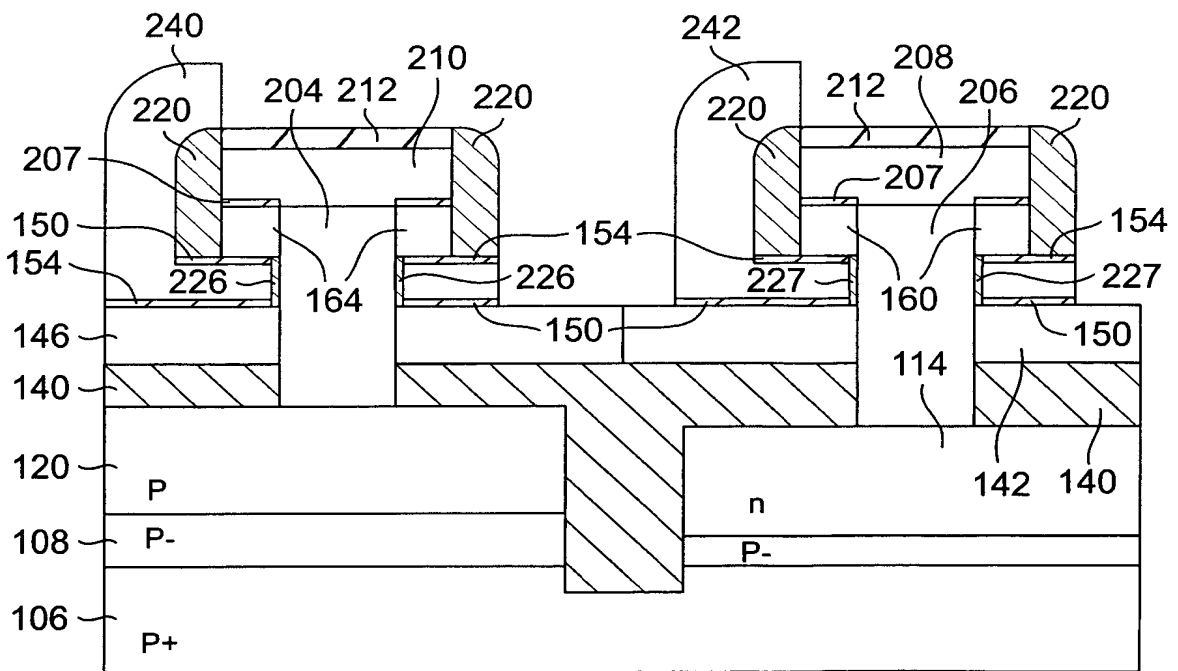


FIG. 33

FIG. 40

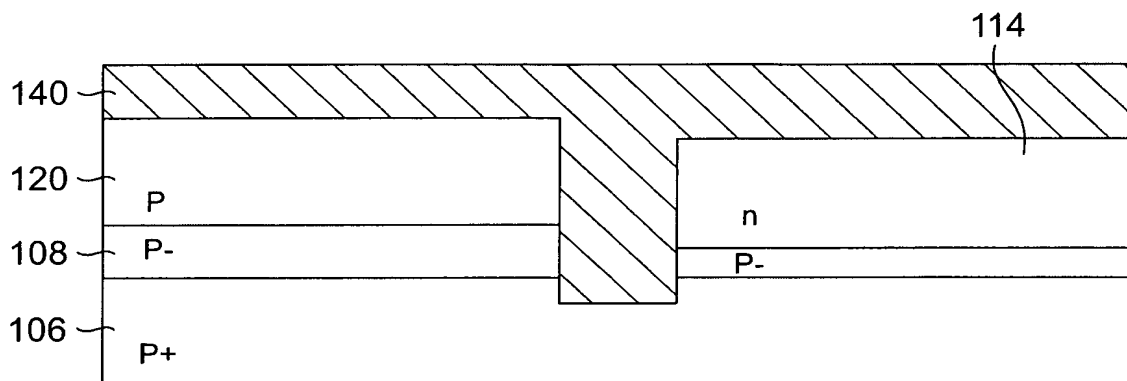


FIG. 35

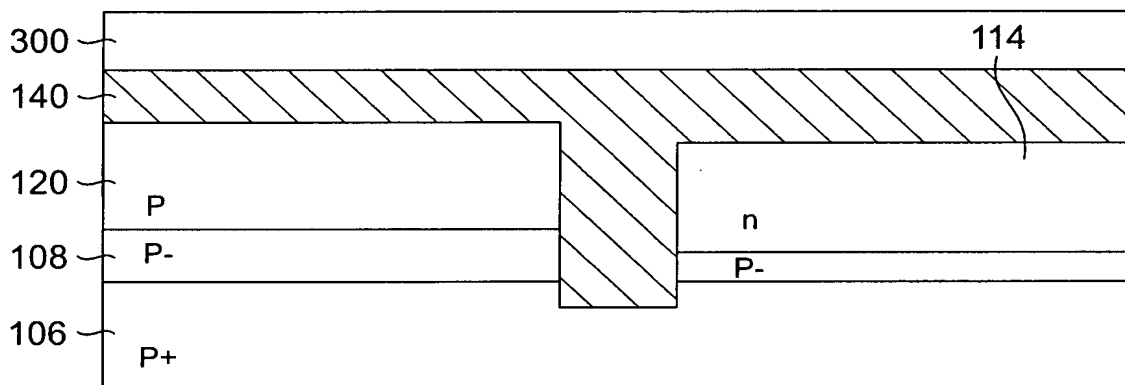


FIG. 36

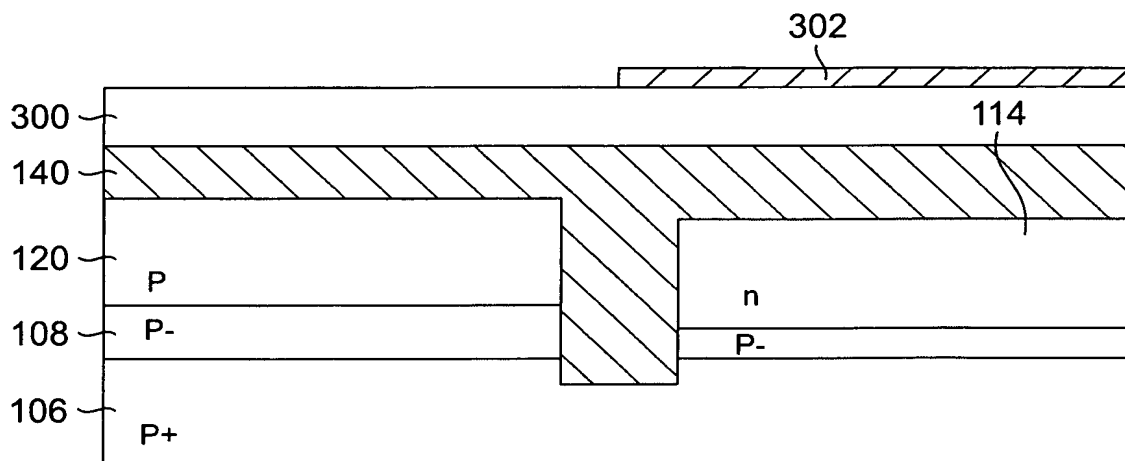


FIG. 37

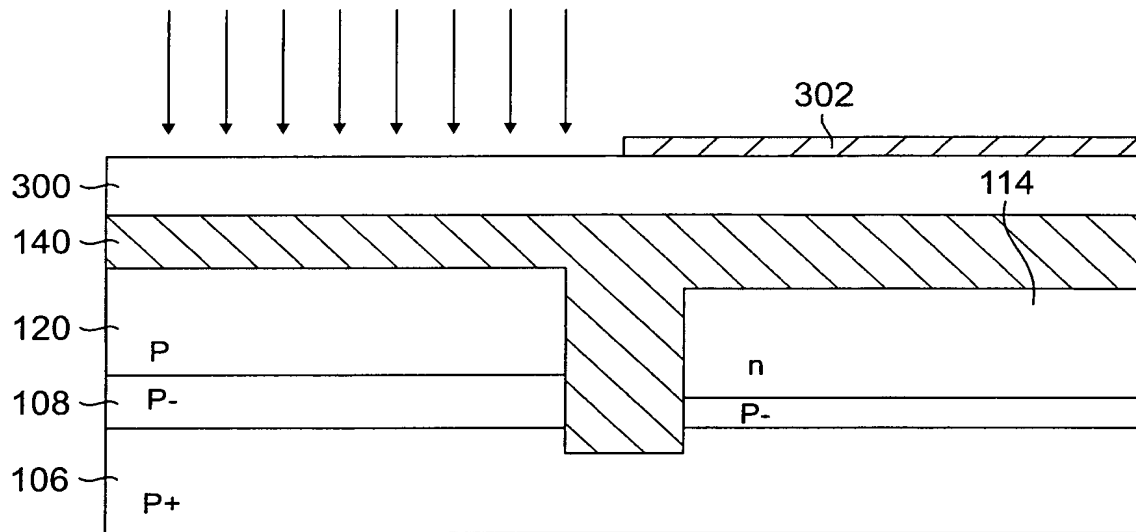


FIG. 38

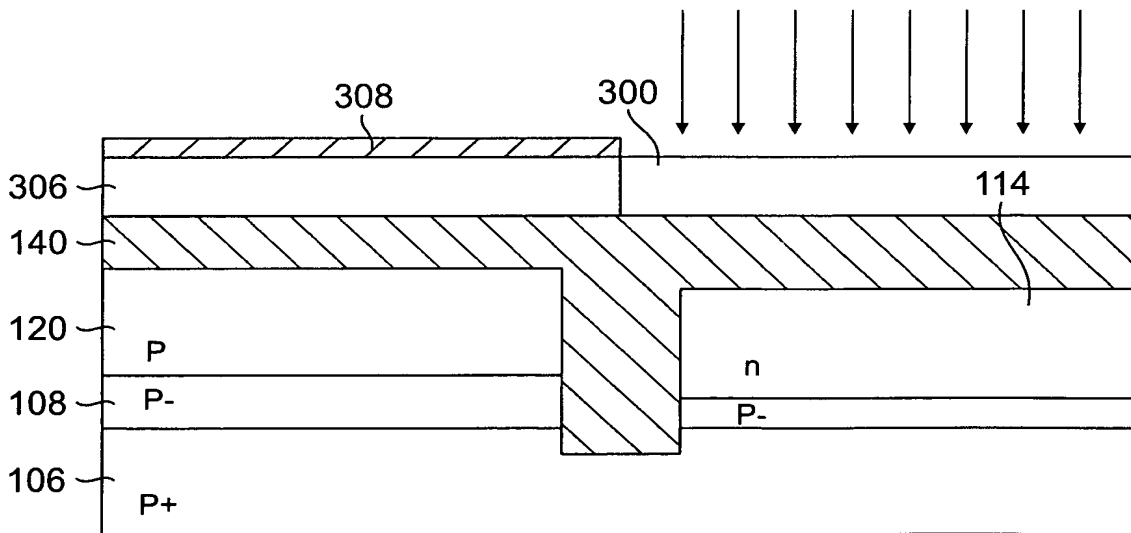


FIG. 39

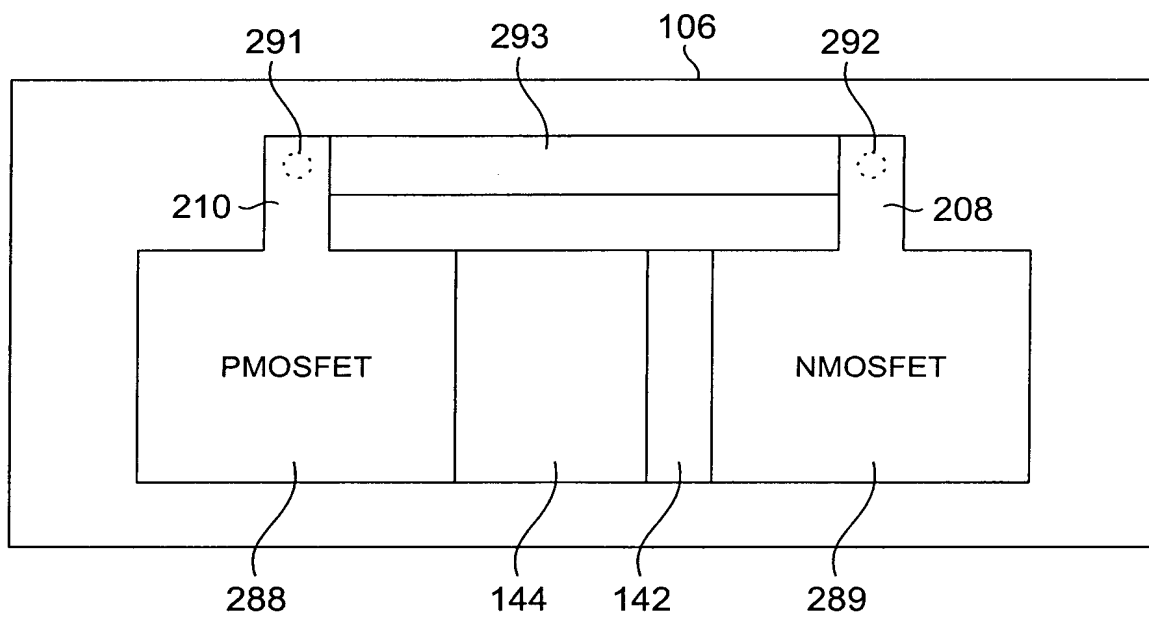


FIG. 41